What is claimed is:

1. A flash memory device with selective gate within a substrate, comprising:

a substrate;

a floating gate disposed on the substrate;

a wordline extending along a first direction and overlying the floating gate and the adjacent substrate thereof;

a trench disposed in the substrate adjacent to one side of the wordline;

a selective gate vertically disposed in the trench and partially covering the floating gate;

a source region disposed in the substrate adjacent to the other side of the wordline; and

a drain region disposed in the substrate beneath the selective gate.

2. The flash memory device as claimed in claim 1, wherein the floating gate further comprises a first dielectric layer and a first polysilicon layer, sequentially stacked on the substrate.

3. The flash memory device as claimed in claim 2, further comprising an oxide layer with a width between 130Å and 220Å disposed on both sides of the first polysilicon layer such that one thereof contacts the selective gate.

4. The flash memory device as claimed in claim 1, further comprising a control gate formed by the portion of the wordline overlying the floating gate.

5. The flash memory device as claimed in claim 1, wherein the wordline extends along a first direction is composed of a second dielectric layer, a second conductive layer and a cap layer.

6. The flash memory device as claimed in claim 5, further comprising a spacer disposed on both sides of the cap layer.

7. The flash memory device as claimed in claim 1, wherein the selective gate further comprises a third dielectric layer and a third conductive layer, and the third dielectric layer formed on one sidewall and portions of the bottom of the trench.

8. The flash memory device as claimed in claim 1, wherein the trench extends along a first direction and has a depth between 800Å and 1200Å.

9. The flash memory device as claimed in claim 7, wherein the third dielectric layer is between 120Å and 200Å.

10. The flash memory device as claimed in claim 7, wherein the third conductive layer is between 200Å and 500Å.

11. A method of fabricating a flash memory device with selective gate within a substrate, comprising the steps of:

providing a substrate;

sequentially depositing a first dielectric layer and a first conductive layer on the substrate;

defining the first conductive layer, to form an active area extending along a first direction;

sequentially depositing a second dielectric layer, a second conductive layer and a cap layer on the substrate, and covering the active area;

defining the cap layer and the second conductive layer, to form a wordline pattern extending along a second direction and partially covering the active area;

forming a pair of spacers respectively disposed on both sides of the wordline pattern to form a wordline;

etching the second dielectric layer and the first conductive layer exposed by the wordline, to form a control gate within the portion of the wordline in the active area;

etching the substrate at one side of the wordline to form a trench therein;

forming a drain region in the substrate beneath the trench;

sequentially forming a third dielectric layer and a third conductive layer on one sidewall and portions of the bottom of the trench, and

partially covering the floating gate, to vertically form a selective gate in the trench; and

forming a source region in the substrate at the other side of the wordline, and electrically contacting the floating gate.

12. The method as claimed in claim 11, wherein the method for forming the third dielectric layer is thermal oxidation.

13. The method as claimed in claim 12, wherein when forming the third dielectric layer, an oxide layer is formed on both sides of the second conductive layer within the floating gate.

14. The method as claimed in claim 13, wherein the oxide layer has a thickness between 130Å and 220Å.

15. The method as claimed in claim 11, wherein the trench has a depth between 800Å and 1200Å.

16. The method as claimed in claim 11, wherein the first direction is substantially perpendicular to the second direction.

17. The method as claimed in claim 11, wherein the third dielectric layer is formed on the sidewall and portions of the bottom of the trench.